Adaptive Antenna Receiver Module for WLAN at C-Band With Low-Power Consumption

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***Abstract*—A low-power consuming adaptive antenna receiver module at C-band for 802.11a and HIPERLAN is presented. The highly integrated GaAs microwave monolithic integrated circuit consists of low noise amplifiers, calibration switches and a vector modulator with 360° phase control and over 15-dB gain control. At 5.2 GHz, the module has a maximum gain of 12.5 dB, a noise figure of 2.7 dB, and a 1-dB output compression point of −7 dBm. The module draws only 2.3 mA up to 3.5 mA from a 2.7 V supply. Chip size is 1.9 mm × 1.6 mm.**

***Index Terms*—Adaptive antenna combining, HIPERLAN, microwave monolithic integrated circuits, wireless local area networks, 802.11a.**

I. Introduction

MARKET forecasts prognosticate high chances for wireless local area networks (WLANs), operating in accordance to the 802.11a and high-performance radio LAN (HIPERLAN) standards at C-band [1]. For indoor data communication they have an allocated frequency band from 5.15 to 5.35 GHz. For this frequency band, remarkable microwave monolithic integrated circuits (MMICs) have been reported for transceivers with single receive and transmit antennas [2]–[9].

Adaptive antenna combining with several antennas in the radio frequency (RF) path has been proposed to decrease intersymbol interferences (ISIs) and to increase indoor data-rates of WLAN systems [10]. High requirements in terms of performance, power consumption, miniaturization, and costs have to be met for corresponding RF frontends. Adequate MMIC components and a multichip module have been reported in [11]–[13], respectively. In comparison, we present a MMIC receiver module with higher integration level, better performance and lower power consumption. It is optimized for the application in an adaptive antenna receiver frontend as shown in Fig. 1. The module consists of low-noise amplifiers (LNAs), calibration switches and a vector modulator (VM) for gain and phase control.

A commercial GaAs foundry process (Triquint TQTRx) featuring 0.6-μm MESFETs is used for fabrication. The circuits are optimized in HP CDS using our modified TOM II large signal model for the MESFETs [14].

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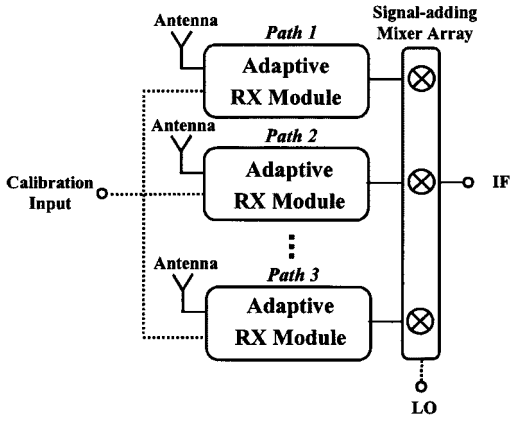

Fig. 1. Adaptive RX frontend. LO: Local oscillator. IF: Intermediate frequency.

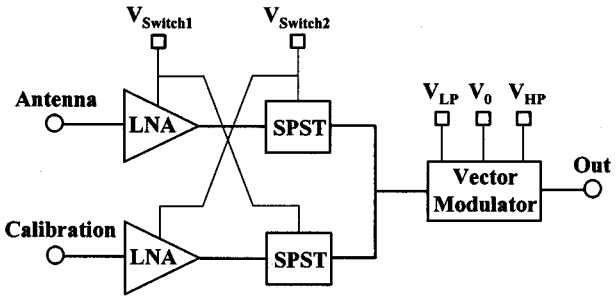

Fig. 2. Circuit schematic of the adaptive RX module. SPST: Single-pole single-throw switch; antenna mode: $V_{\mathrm{Switch1}} = 2.7$ V, $V_{\mathrm{Switch2}} = 0$ V; calibration mode: $V_{\mathrm{Switch1}} = 0$ V, $V_{\mathrm{Switch2}} = 2.7$ V.

II. Design

The circuit schematic of the adaptive antenna receiver (RX) module is shown in Fig. 2. Optionally, it can be switched between the antenna signal and a calibration signal to enable a calibration procedure. This calibration can be applied to decrease effects of process variations, aging, temperature, and frequency changes. b

A. Low Noise Amplifiers

The circuit schematic of the LNAs is shown in Fig. 3. Low power consuming enhancement FETs (E-FETs) in cascode configuration are used. A bias stabilization circuit is applied to decrease effects of threshold voltage variations. The LNAs can be switched off by switching off the supply voltage (V_{Control}).

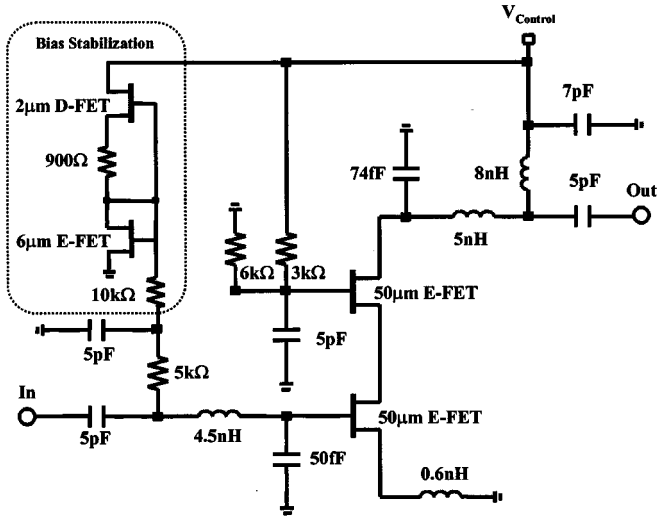

Fig. 3. Circuits schematic of the LNA.

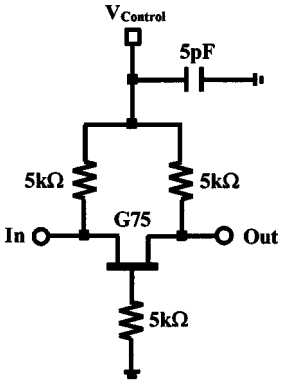

Fig. 4. Circuit schematic of the SPST.

B. Single Pole Single Throw Switches

The circuit schematic of the single-pole single-throw (SPST) switches is shown in Fig. 4. Passive deep depletion FETs (G-FETs) are used as switchable attenuators. At $V_{\mathrm{Control}} = 0$ V, the FET is switched on, whereas at $V_{\mathrm{Control}} = 2.7$ V, the FET is switched off.

C. Vector Modulator

The circuit schematic of the VM is shown in Fig. 5. Gain and 360° phase control is obtained by weighting the gain of the three paths with phase offsets of 120°.

The gains can be controlled by the control voltages $(V_{\mathrm{LP}}, V_0, V_{\mathrm{HP}})$ of the variable gain amplifiers (VGAs) . The analog control voltages can be set by integrated digital to analog converters as reported in [15].

The phase offsets of ±120° are generated by LC high-pass and low-pass filters. The three paths are added by a modified Wilkinson combiner using lumped elements.

III. Results

A photography of the module is shown in Fig. 6. It has a chip size of 1.9 mm × 1.6 mm. All measurements were performed at a supply voltage of 2.7 V. For testing, the LNAs, the switches

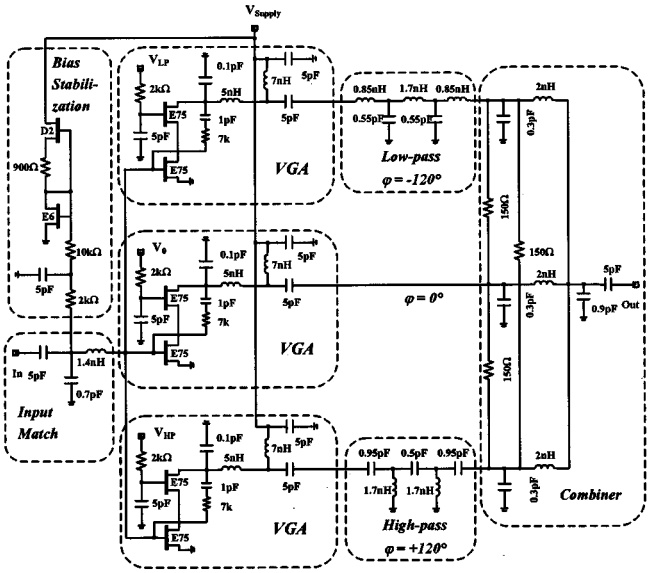

Fig. 5. Circuit schematic of the vector modulator.

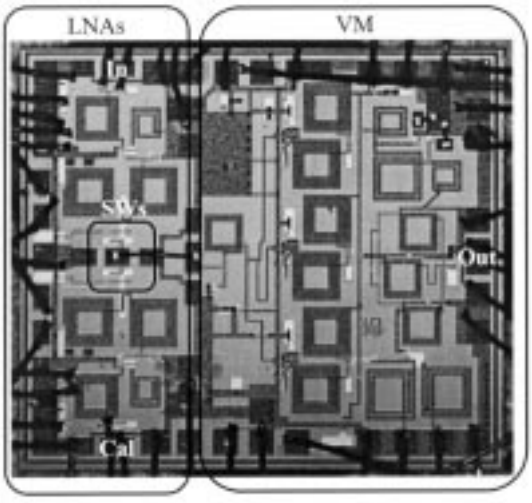

Fig. 6. Photograph of the RX MMIC module. Chip size is 1.9 mm × 1.6 mm. SWs: Switches.

and the VM were also fabricated as stand-alone circuits. Corresponding results, measured on-wafer at 5.2 GHz are listed in Tables I, II, and III, respectively. The module was mounted and bonded on a $1'' \times 1''$ duroid substrate, having input and output losses of approximately 0.2 dB. The results are summarized in Table IV.

The current consumption of one LNA and one VGA is only 1.1 mA and 1.2 mA, respectively. Therefore, the minimum and maximum current consumption of the module is 2.3 mA and 3.5 mA, respectively. Note that only one LNA and one up to two VGAs are working at the same time. Within 5.15 to 5.35 GHz, the maximum gain of the module is higher than 12 dB, as shown in Fig. 7. The VGAs of the VM have a high gain control range of over 32 dB. Within 5.15 to 5.35 GHz, phase offsets between the different VM paths of 120° ± 3° are measured. A phase control range of 360° is obtained by weighting the gains of the three paths. A noise figure smaller than 2.8 dB and an output compression point higher than −7 dBm were measured for the

TABLE I
ON-WAFER MEASUREMENTS LNAS AT 5.2 GHZ

Gain	14dB
Noise figure	1.9dB
Attenuation in off-mode	33dB
$P_{-1dB, Out}$	-7dBm
OIP3	1dBm
DC power consumption	1.1mA at 2.7V
Chip area	$0.5mm^2$

TABLE II
ON-WAFER MEASUREMENTS SWITCHES AT 5.2 GHZ

Loss	1.7dB
Attenuation in off-mode	20dB
Chip area	$<0.1mm^2$

TABLE III
ON-WAFER MEASUREMENTS VM AT 5.2 GHZ

Gain control	-15dB..0.5dB
Phase control	0°..360°
$P_{-1dB, Out}$	-6dBm
OIP3	3dBm
DC power consumption	1.2mA..2.4mA at 2.7V
Chip area	$2mm^2$

TABLE IV
MEASURED RESULTS OF THE MODULE

Bandwidth	5.15GHz-5.35GHz
Gain control	-20dB..12dB
Phase control	0°..360°
Noise figure	<2.8dB
$P_{-1dB, Out}$	-7dBm
OIP3	0dBm
Isolation of switches	>50dB
Total power consumption	2.3mA..3.5mA at 2.7V
MMIC technology	0.6µm GaAs MESFET
Chip size	1.9mm x 1.6mm
MMIC costs in mass-fabrication	<2US$
Applications	Adaptive Antennas, WLAN, HIPERLAN, 802.11a

module within 5.15 to 5.35 GHz. The isolation of the calibration signal in the antenna mode and the isolation of the antenna signal in the calibration mode is 50 dB. One LNA is switched off together with one SPST switch. The GaAs chip costs of the MMIC module in mass-fabrication are less than $2 (U.S.).

IV. CONCLUSION

An adaptive antenna frontend at C-band has been presented. The compact and highly integrated GaAs MMIC module consists of LNAs, calibration switches, and a vector modulator for phase and gain control. A calibration can be applied to decrease effects of process variations, temperature changes, and aging.

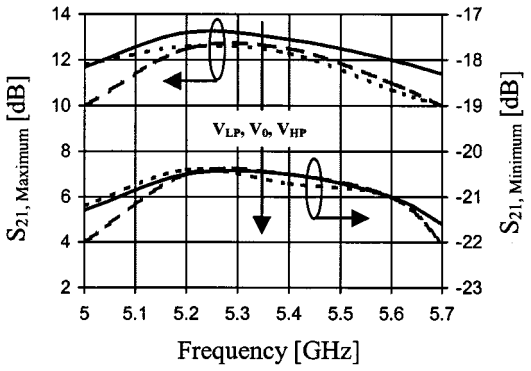

Fig. 7. Maximum gain and minimum gain of the different paths of the module, when the other two paths are switched off.

The low-power consumption and the moderate costs make the module very well suited for wireless applications according to the 802.11a and HIPERLAN standards.

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